Abstract

In order to enable high speed, high bandwidth data transfer between two ASIC devices, for example in a backplane, a wide parallel input data word is divided into a smaller number of words, and each smaller word is converted to serial form and then transmitted over a respective sub-link at a high clock rate relative to the system clock. At the receiving side, the clock is recovered from the serial words, and the serial words are converted back to parallel form. An alignment process is then carried out, firstly involving detecting the positions of the bits of the words and then storing the words in a buffer FIFO register. The words are clocked out of the FIFO register in synchronism under control of the system clock once it is detected that valid words are received in the FIFO registers.

UNITED STATES PATENT AND TRADEMARK OFFICE
DOCUMENT CLASSIFICATION BARCODE SHEET

Drawings

7

Level - 2
Version 1.1

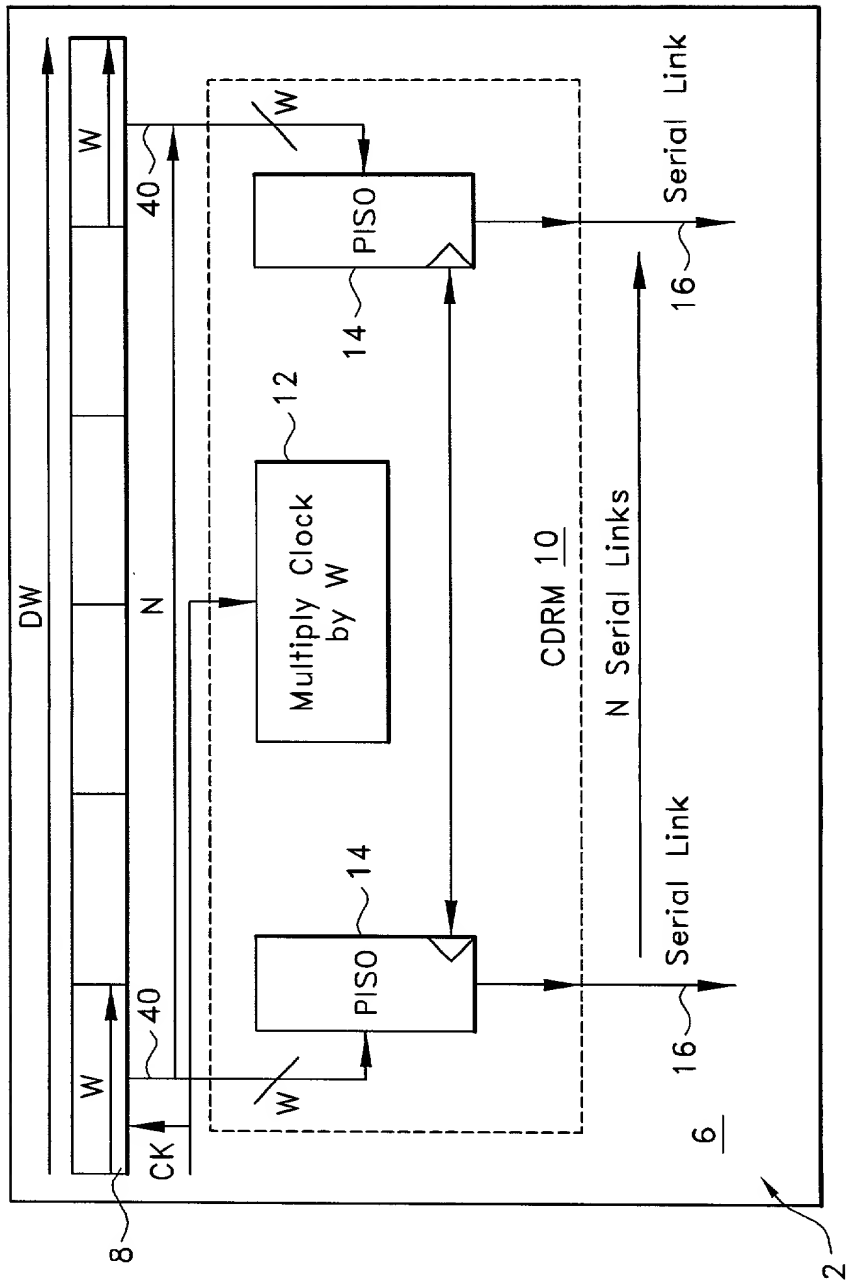


FIG. 1

FIG. 2

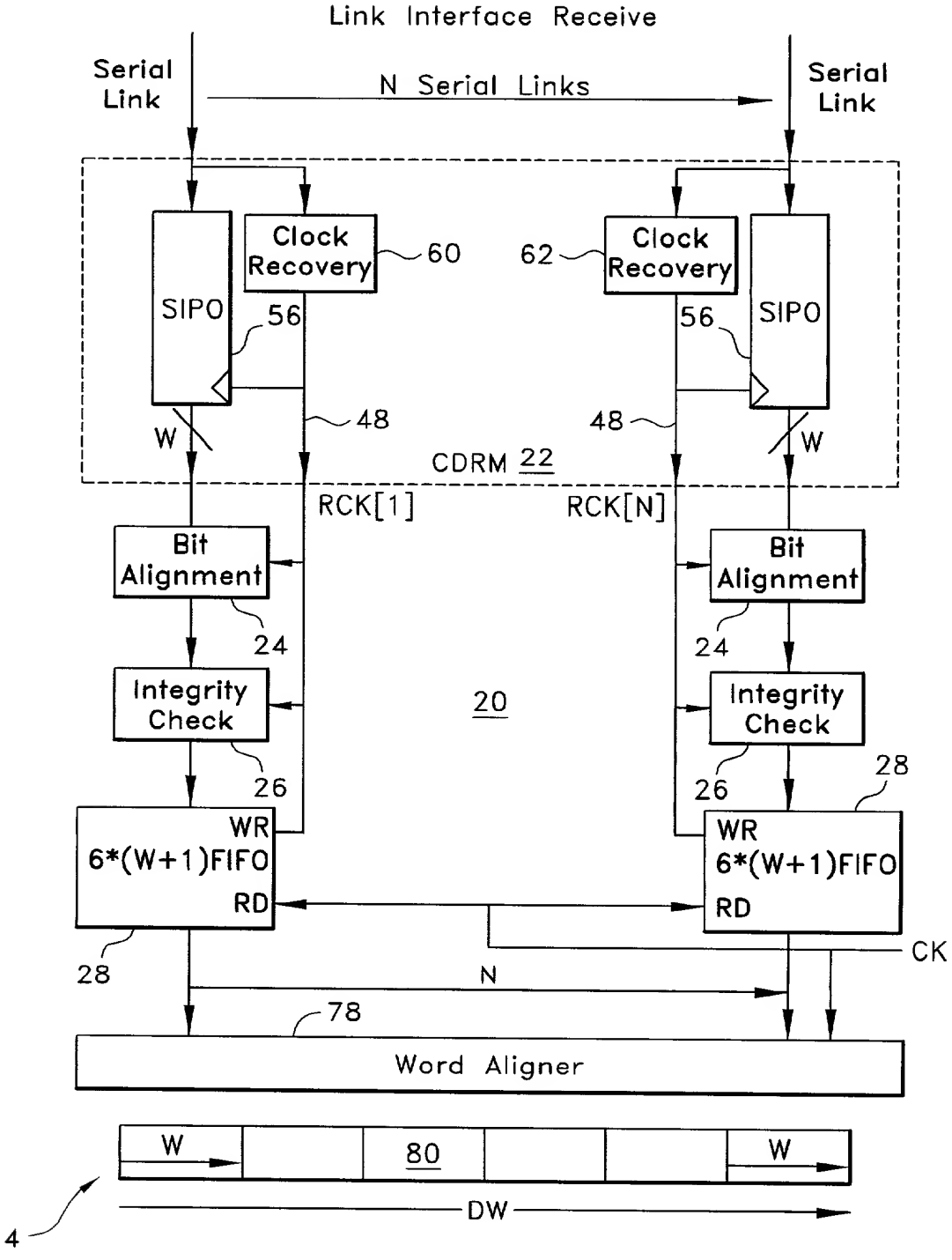

Link Interface Receive
Serial Link
N Serial Links
Serial Link
SIPO
Clock Recovery
60
62
Clock Recovery
56
56
SIPO
48
48
W
W
CDRM 22
RCK[1]
RCK[N]
Bit Alignment
Bit Alignment
24
24
Integrity Check
20
Integrity Check
26
26
28
WR
6*(W+1)FIFO
RD
WR
6*(W+1)FIFO
RD
CK
28
N
78
Word Aligner
W
80
W
DW
4

FIG. 3 Word Aligner Trigger

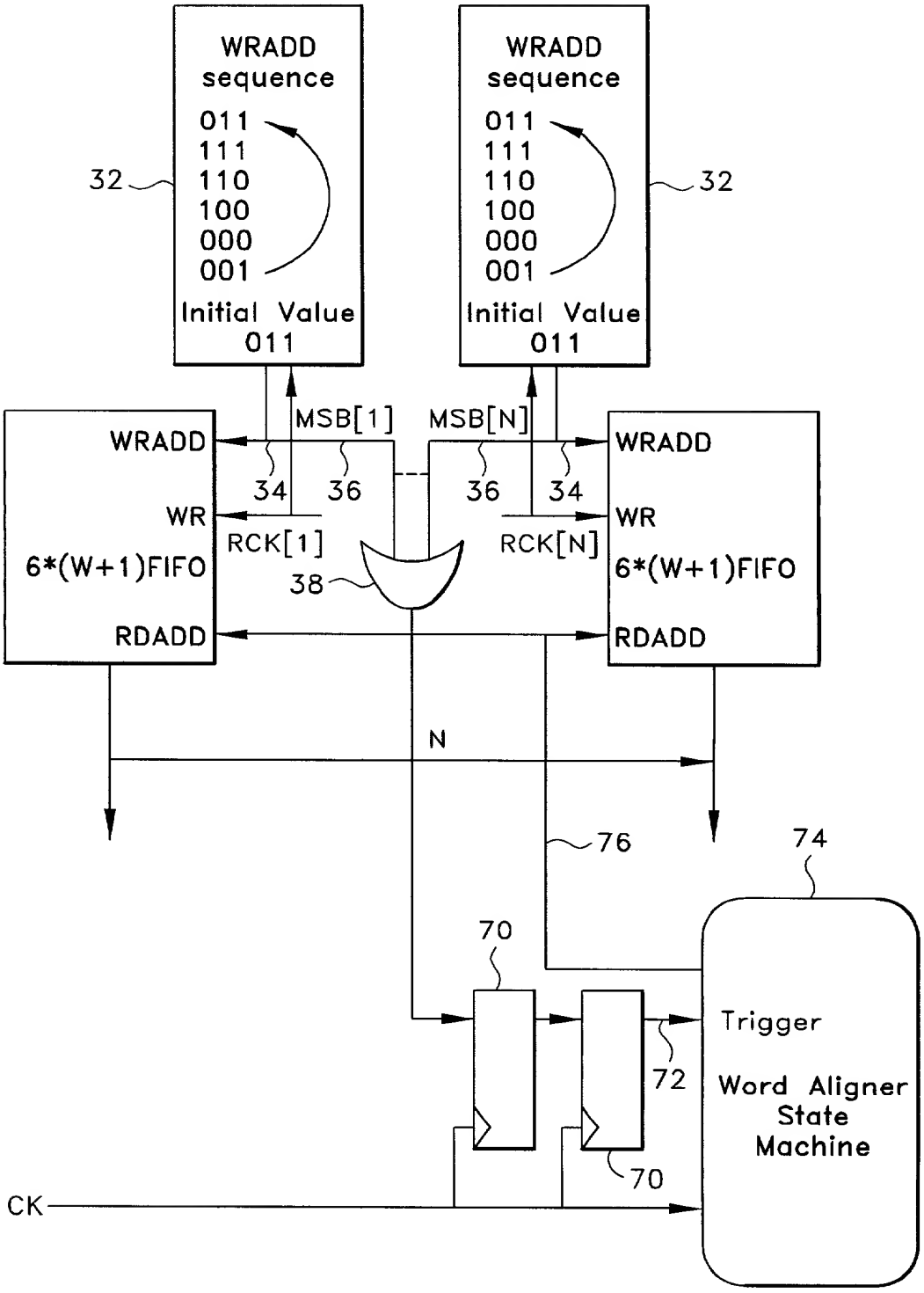
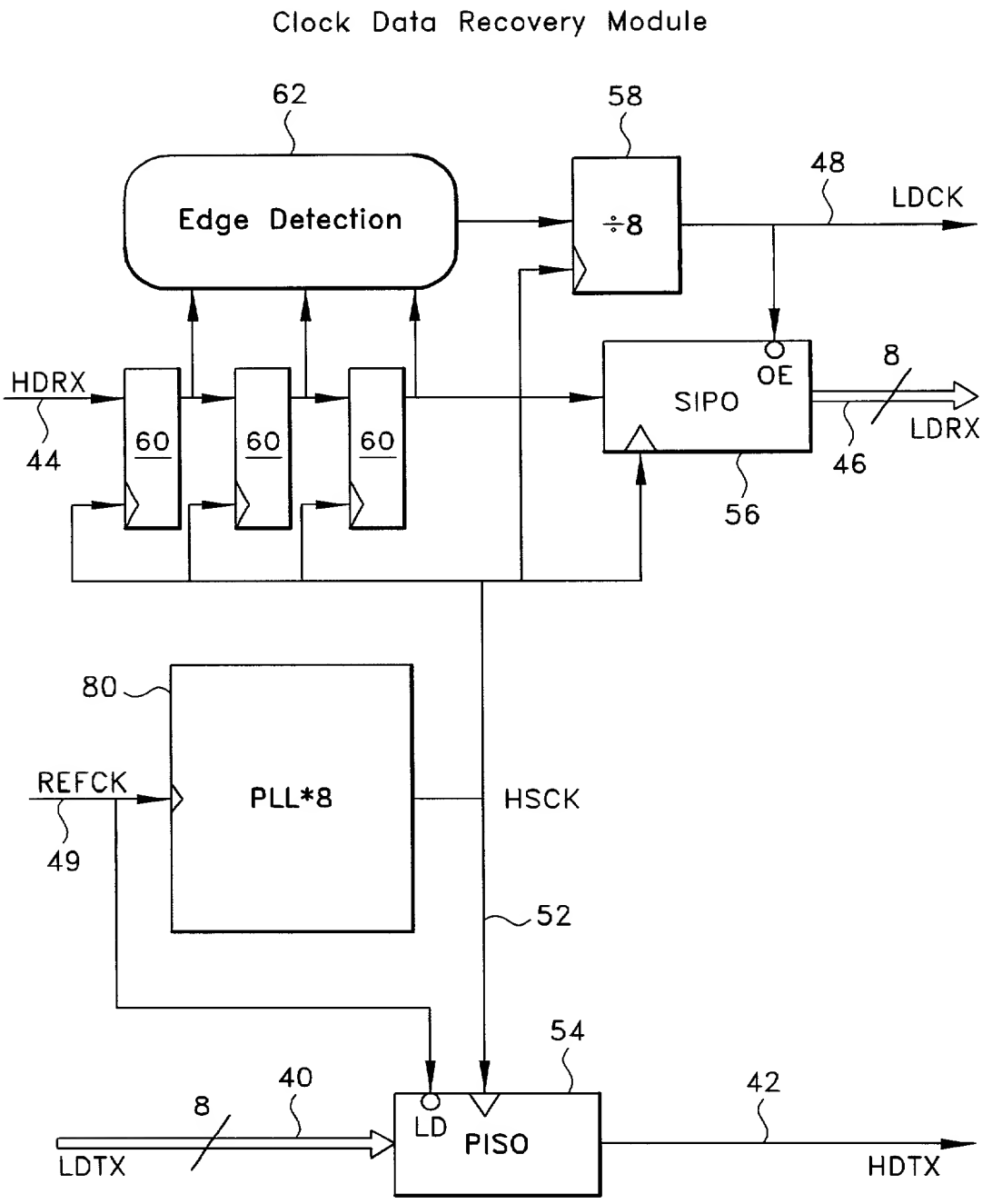


FIG. 4


Clock Data Recovery Module
62
58
48
LDCK
Edge Detection
÷8
HDRX
44
60
60
60
SIPO
OE
8
LDRX
46
56
80
REFCK
49
PLL*8
HSCK
52
54
40
8
LDTX
LD
PISO
42
HDTX